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EXAMINER	
HERNANDEZ, NELSON D	
ART UNIT	PAPER NUMBER
2612	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/643,800	KAWASE ET AL.	
	Examiner	Art Unit	
	Nelson D. Hernandez	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 August 2000 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3-8 and 4/9/2000.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 4, 7, 8 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada, US Patent 6,456,324 B1.

Regarding claim 1, Yamada discloses an electronic camera (First embodiment, Fig. 1) comprising: an image-sensing unit (Fig. 1: 2) for electronically sensing an object image and outputting image data of the object image; a memory unit (Fig. 1: 4) for storing the image data output from said image sensing unit; an image processing unit (Fig. 1: 5) for performing predetermined image processing based on the image data stored in said memory unit; an interpolation calculation circuit (Fig. 1: 6) for interpolating a pixel whose data is not present in the image data after image processing by said image processing unit by interpolation calculation based on an approximate expression including a polynomial of at least 3rd-order (Col. 7, line 66 – col. 8, line 18; col. 9, lines 43-65), Yamada also teaches a recording unit for recording the image data after interpolation on a recording medium (Fig. 1: 10) (Col. 7, lines 12-18). Yamada also discloses the use of a display unit for displaying the images data after interpolation (Col. 1, lines 28-39).

In another embodiment (Fig. 20), Yamada teaches the image stored at the memory unit (Fig. 20: 54) memory being interpolated by the interpolation processing circuit (Fig. 20: 55) and writing the image data after interpolation in said memory unit (Col. 29, lines 1-11 and lines 46-61).

Therefore it would have been obvious to one of ordinary skilled in the art to have the image interpolated by the interpolation processing circuit (First embodiment) stored back in the image memory with the motivation of overwriting the image prior to interpolation stored in the image memory as taught by Yamada (Second embodiment). Doing so would help the electronic camera to free memory space.

Regarding claim 3, Yamada discloses that the interpolation calculation is a convolution calculation based on an approximate expression including a 3rd-order (cubic) polynomial (Col. 9, lines 53-65; col. 29, lines 46-61).

Regarding claim 4, Yamada inherently teaches that the memory unit (Fig. 20: 54) has a memory area dedicated for the interpolation calculation by said interpolation calculation circuit by teaching that the interpolated image is stored back in the memory unit (Col. 29, lines 1-11).

Regarding claim 7, Yamada discloses the image-sensing unit (Fig. 1: 2 and fig. 20: 52) comprising a single image-sensing element (single-CCD) to which an optical filter (Fig. 12) having an RGB color coating is attached (Col. 21, lines 44-65).

Regarding claim 8, Yamada teaches a color separation unit (Fig. 1: 9 and fig. 20: 59) for separating pixels in units of RGB color components based on a form of the color coating of said image sensing element to generate pixel planes of the RGB color

components from one pixel plane, and wherein said interpolation calculation circuit interpolates the pixel whose data is not present in the pixel planes of the RGB color components (Col. 8, lines 9-18; col. 9, lines 53-65; col. 29, lines 1-11).

Regarding claim 12, Yamada inherently teaches that the electronic camera comprises an address control unit for controlling a write address in writing the image data processed by said image processing unit in said memory unit, wherein said address control unit overwriting part of the image data on part of image data which has already been written by disclosing that the original image signals before the light-quantity difference correction in the image memory are erased since the original image signals after the light-quantity difference correction are overwritten thereon (Col. 7, line 66 – col. 8, line 8).

Regarding claim 13, Yamada teaches the address control unit to control an offset address from a start address of a storage area of said memory unit by teaching determining addresses to which pieces of pixel data of the images are alternately stored and storing them in the corresponding addresses so as to superimpose the images in a manner so as to offset said images form each other (Col. 9, lines 15-34).

3. Claims 2, 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada, US Patent 6,456,324 B1 in view of Takezawa, US 2003/0147634 A1.

Regarding claim 2, Yamada does not explicitly disclose a compression/expansion unit for compressing the image data after image processing or expanding the image data read out from said recording unit.

However, Takezawa teaches a compression/expansion unit (Fig. 1: 208 and fig. 2: 28) for compressing the image data after image processing or expanding the image data read out from a recording unit (Fig. 1: 209 and fig. 2: 32) (Page 1, ¶008; page 2, ¶0041).

Therefore, taking the combined teaching of Yamada in view of Takezawa as a whole, it would have been obvious to one of ordinary skilled in the art to modify Yamada by incorporating a compression/expansion unit for compressing the image data after image processing or expanding the image data read out from a recording unit. The motivation to do so would help the electronic camera to display the expanded image on a display as taught by Takezawa (Page 1, ¶ 0008).

Regarding claim 5, Yamada does not explicitly disclose a dedicated memory unit used for the interpolation calculation by said interpolation calculation circuit.

However, Takezawa teaches the use of buffer memories (Fig. 6, items 72 and 74) for conducting an image interpolation process by a resolution conversion circuit (Fig. 6: 28) (Page 6, ¶ 0090).

Therefore, taking the combined teaching of Yamada and Takezawa as a whole, it would have been obvious to one of ordinary skilled in the art to modify Yamada by incorporating buffer memories dedicated to the interpolation process with the motivation of process the images with the motivation of buffering the image data to be vertical and horizontal interpolated individually as suggested by Takezawa (Page 6, ¶ 0090).

Regarding claim 11, Yamada does not explicitly disclose that the image processing includes thinning of predetermined pixels and format conversion based on a

sum of the predetermined pixels, and said interpolation calculation circuit interpolates the pixel whose data is not present in the image after the format conversion.

However, Takezawa teaches that the CCD image sensor has a function of thinning out image signals and is able to thin out vertical components of the image signals to $1/2, 1/3, 1/4, \ldots$ to output the resulting thinned-out signals (when thinning out the image signal is performing a format conversion), also teaches conducting an image interpolation process by a resolution conversion circuit on the image stored in the memory unit (Page 3, ¶0038; page 6, ¶ 0090).

Therefore, taking the combined teaching of Yamada in view of Takezawa as a whole, it would have been obvious to one of ordinary skilled in the art to modify Yamada by performing thinning out of the image signals and to make interpolation on the image thinned out. The motivation to do so would enable the electronic camera to reduce the amount of data when formatting images as suggested by Takezawa (Page 3, ¶0038).

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada, US Patent 6,456,324 B1 in view of Ogata, US Patent 6,753,910 B1.

Regarding claim 6, Yamada teaches that the interpolation calculation circuit comprises: a calculation section for calculating an interpolation position of a pixel (Col. 7, line 66 – col. 8, line 18) but does not explicitly teach an interpolation coefficient table storing an interpolation coefficient; a correction section for correcting the interpolation position so as to correspond to the interpolation coefficient; and an interpolation calculation section for interpolating the pixel using the interpolation coefficient for the corrected interpolation position.

However, Ogata teaches the use of a lookup table (Fig. 11: 51) to store a correction coefficient corresponding to a predetermined pixel location to be used by the interpolation circuit (Fig. 11: 52) (Col. 11, lines 36-67).

Therefore, taking the combined of Yamada in view of Ogata as a whole, it would have been obvious to on of ordinary skilled in the art to modify Yamada by incorporating a lookup table to calculate a correction coefficient corresponding to a predetermined pixel location to be used by the interpolation circuit. Doing so would help the electronic camera to perform gradiation correction as suggested by Ogata (Col. 11, lines 16-34).

5. Claims 9, 10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada, US Patent 6,456,324 B1 in view of Hieda, US 2001/0043760 A1.

Regarding claims 9 and 10, Yamada does not explicitly teach that the image processing includes enlargement and reduction of an image, and wherein said interpolation calculation circuit interpolates the pixel whose data is not present in the enlarged or reduced image.

However, Hieda teaches an image pick up apparatus (Figs. 12A and 12B), wherein image interpolation circuits (Fig. 12B: 213, 214, 217, 218) perform image enlargement/reducing using an interpolation coefficient generated (Fig. 12A: 222 and 223) based on a magnification factor input (Fig. 12A: 221). Hieda also teaches that the interpolated signals are output to a recorder unit or a display (Page 6, ¶0112, 0116 and 0120). By enlarging an image using interpolation, the image interpolation circuit calculates image data for a predetermined number of pixels depending on the magnification selected by the user.

Therefore, taking the combined teaching of Yamada in view of Hieda, it would have been obvious to one of ordinary skilled in the art to modify Yamada by enlarging or reducing the images based on a magnification factor so as to output said interpolated images to a recorder unit or a display unit. The motivation to do so would help the electronic camera to provide enlarge or reduced images with high image quality with improvement in image definition as suggested by Hieda (Page 1, ¶0019).

Regarding claim 17, Yamada does not explicitly teach an image quality mode-setting unit for setting an image quality mode of the sensed image, and wherein only when the image quality mode with a variable image size is set, the interpolation calculation by said interpolation calculation circuit is performed.

However, Hieda teaches Hieda teaches an image pick up apparatus (Figs. 12A and 12B) having an image enlargement/reduction selection circuit having a high quality image interpolation circuit that

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada, US Patent 6,456,324 B1 in view of Yasuda, US 2001/0010558 A1.

Regarding claim 14, Yamada does not explicitly discloses that the electronic camera comprises at least one of an automatic focus control unit and an automatic exposure unit, and wherein the interpolation calculation circuit executes the interpolation calculation when said automatic focus control unit and said automatic exposure unit are an inoperative state.

However, Yasuda teaches an image pick up apparatus (Fig. 2) comprising an auto focus control unit (Fig. 2: 111) for controlling the focusing lens position so as to

take a frame and store said frame in a field memory (Fig. 2: 114), then the interpolation circuit (Fig. 2: 115) is arranged to read the signal out from the field memory (Page 2, ¶ 0034). Furthermore, Yasuda teaches the use and operation of an automatic exposure circuit for another embodiment (Fig. 7; page 3, ¶0044).

Therefore, taking the combined teaching of Yamada and Yasuda as a whole, it would have been obvious to one of ordinary skilled in the art to modify Yamada by integrating an automatic focus control to control the focusing lens position prior to capture a frame. The motivation to do so would help the electronic camera to carry out an automatic focus control and an automatic exposure control without blurring images even when an image is magnified by varying the aspect ratio of the image plane (Page 1, ¶ 0011).

Regarding claim 14, Yamada does not explicitly disclose at least one of an automatic focus control unit and an automatic exposure unit, and wherein said interpolation calculation circuit executes the interpolation calculation when said automatic focus control unit and said automatic exposure unit are in an inoperative state.

7. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada, US Patent 6,456,324 B1 in view of Nobuoka, US Patent 6,031,569.

Regarding claims 15 and 16, Yamada does not explicitly teaches an image sensing mode setting unit for setting an image sensing mode, and wherein whether execution of the interpolation calculation by said interpolation calculation circuit is

enabled/disabled is determined in correspondence with the image sensing mode set by said image sensing mode setting unit.

However, Nobuoka teaches and image sensing apparatus having selecting means for selecting one of a plurality of operational modes, normal moving picture mode and still picture mode, wherein said image sensing apparatus perform interpolation to obtain color components (Col. 3, lines 15-26; col. 7, lines 45-67).

Therefore, taking the combined teaching of Yamada in view of Nobuoka as a whole, it would have been obvious to one of ordinary skilled in the art to modify Yamada by incorporating a selecting means for selecting one of a plurality of operational modes. Doing so would help the electronic camera to obtain both high-resolution still images and motion pictures without losing the merits of compactness and inexpensive single image sensor type image sensing apparatus as suggested by Nobuoka (Col. 1, lines 60-65).

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada, US Patent 6,456,324 B1 in view of Fellegara, US 2001/0015760 A1.

Regarding claim 17, Yamada does not explicitly disclose that the electronic camera comprises an image quality mode setting unit for setting an image quality mode of the sensed image, and wherein only when the image quality mode with a variable image size is set, the interpolation calculation by said interpolation calculation circuit is performed.

However, Fellegara teaches an electronic camera comprising an image capture mode (Page 6, ¶0053) and a zoom/focus mechanism (Fig. 6: 82) for controlling the

zoom when operating the electronic camera (Page 6, ¶0052), wherein the image resolution is varied based on the image capture mode selected, Fellegara also teaches that the interpolation is performed on the full resolution images for applying the selected capture modes (Page 6, ¶0053).

Therefore, taking the combined teaching of Yamada in view of Fellegara as a whole, it would have been obvious to one of ordinary skilled in the art to modify Yamada by incorporating an image capture mode so as to modify the resolution of the image to be captured. The motivation to do so would help the electronic camera to change the resolution of the images captured according to a selected capture mode (i.e. film, hybrid, quick review) as suggested by Fellegara (Page 6, ¶0053).

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson D. Hernandez whose telephone number is (703) 305-8717. The examiner can normally be reached on 8:30 A.M. to 6:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nelson D. Hernandez
Examiner
Art Unit 2612

NDHH

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PRIMARY EXAMINER